IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT

APPEALS AND INTERFERENCES

In Re Application of:	)
Kenneth Koch II et al.	)Atty Dkt. 10017912-3
Serial No.: 10/777,902	) Group Art Unit: 2816
Filed: February 13, 2004	) Examiner: Terry Lee Englund

For: DRIVER CIRCUIT CONNECTED TO A SWITCHED CAPACITOR AND METHOD OF OPERATING SAME

APPEAL BRIEF

Mail Stop Appeal Brief - Patents

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief is submitted in response to the Final Rejection of the claims mailed February 5, 2009. A Notice of Appeal was filed on April 13, 2009.

This brief contains items under the following headings as required by 37 CFR §41.37 and MPEP §1206:

(1) Real Party In Interest
(2) Related Appeals and Interferences
(3) Status of Claims
(4) Status of Amendments
(5) Summary of Claimed Subject Matter
(6) Grounds of Rejection to be Reviewed on Appeal
(7) Argument
(8) Claims Appendix
(9) Evidence Appendix
(10) Related Proceedings Appendix

(1) REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, LP, a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

(2) RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences currently known to appellant, appellant's legal representatives or the assignee, which will directly affect, or be directly affected by, or have a bearing on, the Board's decision.

(3) STATUS OF CLAIMS

Claims 1-24 were filed with the application. Claims 3-4, 6, 8, 9, 11-22 and 24-31 are currently pending in the application. Claims 1-2, 5, 7, 10 and 23 are canceled. Claims 22 and 24 are allowed. The rejection of claims 3-4, 6, 8, 9, 11-21 and 25-31 is appealed.

(4) STATUS OF AMENDMENTS

No amendments were filed or entered subsequently to the Final Office Action mailed February 5, 2009.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

Appellants' invention as independently claimed is summarized and explained below with reference numerals, specification page numbers and drawing figure numbers indicating where the claim finds support in the specification and drawings.

22. A method of operating a driver (10) including first (48) and second (50) opposite conductivity type transistors, each including a control electrode (28 &30) and a path between a pair of further electrodes controlled in response to a voltage applied to the control electrode, the paths of the first (48) and second (50) transistors being connected in series across opposite first (18) and second (16) power supply terminals, an output terminal (26) between the series connected paths, a first switchable capacitor (32) connected between the control electrode (28) of the first transistor (48) and the first power supply terminal (18) and a second switchable capacitor (34) connected between the control electrode (30) of the second transistor (50) and the second power supply terminal (16), the method comprising [Fig. 1; pg. 9, lines 15-16; pg. 10, lines 21-23]:

during a first interval: causing the paths of the first (48) and second (50) transistors to be respectively, on and off by applying

[Fig. 1; pg. 10, line 21]

(a) a first voltage having a first value to the control electrode (28) of the first transistor (48) [Fig. 1; pg. 11, lines 1-3] and

(b) a second voltage having the first value to the control electrode (30) of the second transistor (50) and across the second capacitor (34) to charge the second capacitor (34) [Fig. 1; pg. 11, lines 2-8];

during a second interval: causing the paths of the first (48) and second (50) transistors to be off and on, respectively, by applying [Fig. 1; pg. 11, lines 1-2]

(a) a second value of the first voltage to the control electrode (28) of the first transistor (48) [Fig. 1; pg. 11, lines 1-3], and

(b) the second value of the second voltage to the control electrode (30) of the second transistor (50) and across the first capacitor (32) to charge the first capacitor (32) [Fig. 1; pg. 11, lines 2-3];

upon a first transition between the first and second intervals: turning off, without any capacitive delay, the path of the first transistor (48) while maintaining, during said first transition and during an initial portion of the second interval, the path of the second transistor (50) off by changing the first voltage from the first value to the second value while the first capacitor (32) is switched off and the second capacitor (34) is charged [Fig. 1; pg. 11, lines 1-4];

after the initial portion of said second interval and during a second, subsequent portion of the second interval: turning on the path of the second transistor (50) while maintaining the path of the first transistor (48) off by changing the charge on the second capacitor (34) so that the second voltage changes from the first value toward the second value [Fig. 1; pg. 11, lines 1-4];

after the second portion of said second interval and during a third, subsequent portion of the second interval: while maintaining the paths of the second transistor (50) and the first transistor (48) on and off, respectively, switching off the second capacitor (34) to cause the second voltage to reach the second value before a subsequent second transition between the second and first intervals [Fig. 1; pg. 11, lines 1-4];

upon the second transition between the second and first intervals: turning off, without ant capacitive delay, the path of the second transistor (50) while maintaining, during said second transition and during an initial portion of the first interval, the path of the first transistor (48) off by changing the second voltage from the second value to the first value while the second capacitor (34) remains switched off and the first capacitor (32) is charged [Fig. 1; pg. 11, lines 1-4];

after the initial portion of said first interval and during a second, subsequent portion of the first interval : turning on the path of the first transistor (48) while maintaining the path of the second transistor (50) off by changing the charge on the first capacitor (32)

so that the first voltage changes from the second value toward the first value [Fig. 1; pg. 11, lines 1-4]; and

after the second portion of said first interval and during a third, subsequent portion of the first interval: while maintaining the paths of the first transistor (48) and the second transistor (50) on and off, respectively, switching off the first capacitor (32) to cause the first voltage to reach the first value before the subsequent first transition between the second and first intervals [Fig. 1; pg. 11, lines 1-4].

26. A driver (10) having an input terminal adapted to be responsive to a bi-level signal, the driver including first (48) and second (50) opposite conductivity type transistors, each including a control electrode and a path between a pair of further electrodes controlled in response to a voltage applied to the control electrode, the paths of the first (48) and second (50) transistors being connected in series across opposite first (16) and second power (18) supply terminals, an output terminal (26) between the series connected paths, a first switchable capacitor (32) connected to a first connection between the control electrode (28) of the first transistor (48) and the second power supply terminal (18), a second switchable capacitor (34) connected to a second connection between the control electrode (30) of the second transistor (50) and the first power supply terminal (16), the first (48) and second (50) transistors having first and second thresholds between the voltages at the first (16) and second (18) power supply terminals so that the

paths of the first (48) and second transistors (50) are arranged to be on and off in response to the voltages applied to the control electrodes (28 & 30) being on opposite sides of the first and second thresholds thereof, the first (32) and second capacitors (34) respectively having third and fourth thresholds between the voltages at the first (16) and second (18) power supply terminals for causing the capacitors (32 &34) to have finite values and be switched off in response to the voltages across the capacitors (32 & 34) being on opposite sides of the third and fourth thresholds [Fig. 1, pg. 9, lines 15-16, pg. 10, lines 21-23];

the control electrodes (28 & 30) and the capacitors (32 &34) being connected to each other and to the input terminal, the connections of the capacitors (32 & 34) to the control electrode (28 &30) and to the input terminal and the first, second, third and fourth thresholds being such that in response to [Fig. 1; pg. 11, line 4]:

(I) a first transition between the levels of the bi-level signal that extends in a first direction, (a) the second capacitor (34) is switched off and the voltage across the second capacitor (34) and at the control electrode (30) of the second transistor (50) suddenly changes toward the voltage at the second power supply terminal (18) in response to the voltage across the second capacitor (34) crossing the fourth threshold, (b) the first transistor (48) is turned off and remains turned off until after a second transition between the levels of the bi-level signal that extends in a second direction, (c) the first capacitor (32) has finite values until after the second transition,

(d) the second transistor (50) (i) is initially off while the first transistor (48) is off, and (ii) then turns on in response to the voltage across the second capacitor (34) and at the control electrode (30) of the second transistor (50) gradually changing in a direction extending from the voltage at the second power supply terminal (18) toward the voltage at the first power supply terminal (16) and crossing the second threshold, and (iii) stays on until the second transition occurs, wherein (a) occurs after (d)(ii) [Fig. 1, pg. 9, lines 15-16, pg. 10, lines 21-23]; and

(II) the second transition, (a) the first capacitor (32) is switched off and the voltage across the first capacitor (32) and at the control electrode (28) of the first transistor (48) suddenly changes toward the voltage at the first power supply terminal (16) in response to the voltage across the first capacitor (32) crossing the third threshold, (b) the second transistor (50) is turned off and remains turned off until after the first transition, (c) the second capacitor (34) has finite values until after the first transition between the levels of the bi-level signal that extends in a second direction, (d) the first transistor (48) (i) is initially off while the first transistor (48) is off, and (ii) then turns on in response to the voltage across the first capacitor and at the control electrode of the first transistor gradually changing in a direction extending from the voltage at the second power supply terminal (18) toward the voltage at the first power supply terminal (16) and crossing the first threshold, and (iii) stays on until the first transition occurs, wherein (a) occurs after (d)(ii) [Fig. 1, pg. 9, lines

15-16, pg. 10, lines 21-23];

wherein said first switchable capacitor (32) is the only voltage responsive switchable capacitor directly connected to said first connection [Fig. 1; pg. 11, line 4]; and

said second switchable capacitor (34) is the only voltage responsive switchable capacitor directly connected to said second connection [Fig. 1; pg. 11, line 4].

31. A circuit comprising a first terminal for connection to a voltage source having first and second levels and a transition between the levels,

a driver (10) including first (48) and second (50) opposite conductivity type transistors, each including a control electrode and a path arranged to be switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold level, the first (48) and second transistor (50) paths being connected in series across opposite power supply terminals, an output terminal (26) between the paths, and circuitry connected between the first terminal and the control electrodes for causing the first (48) and second transistor (50) paths to be respectively (a) in on and off states while the voltage source has the first level and (b) in off and on states while the voltage source has the second level [Fig. 1; pg. 9, lines 15-16; pg. 10, lines 21-23],

wherein said circuitry includes at least one voltage responsive switchable capacitor connected (a) to be responsive to voltage at the

first terminal and (b) to the driver (for preventing the paths of the first (48) and second (50) transistors from being on simultaneously during transitions between the on and off states of the first and second transistor paths, the at least one switchable capacitor being arranged to have an initial finite capacitance value during an initial part of the transition between the levels and to be switched from the initial finite capacitance value to a substantially open circuit in response to the voltage across the at least one switchable capacitor changing during the transition between the levels from one side of a threshold voltage to a second side of the threshold voltage, the threshold voltage being between the first and second levels [Fig. 1; pg. 11, lines 1-3];

said at least one voltage responsive switchable capacitor has a capacitor control electrode connected to the control electrode of one of the first (48) and second (50) transistors to receive the voltage applied to the control electrode of said one of the first (48) and second (50) transistors [Fig. 1; pg. 11, lines 1-3];

the threshold voltage of said at least one voltage responsive switchable capacitor and the threshold level of said one of the first (48) and second (50) transistors are configured such that, as the voltage changes in a direction to switch said one of the first (48) and second (50) transistors from off to on, said one of the first (48) and second transistors (50) is switched from off to on before said at least one voltage responsive switchable capacitor is switched from the initial finite capacitance value to the substantially open circuit [Fig. 1;

pg. 11, lines 1-3]; and

said at least one voltage responsive switchable capacitor is the only voltage responsive switchable capacitor connected to the control electrode of said one of the first and second transistors.

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 3-4, 6, 8-9, 11-18 and 25-31 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Naganuma (U.S. Patent No. 4,827,159) in view of Bui et al. (U.S. Patent No. 6,201,752).

B. Claims 19-21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Naganuma (U.S. Patent No. 4,827,159) and Bui (U.S. Patent No. 6,201,752) as applied to claim 18 and in view of Yoshizawa et al. (U.S. Patent No. 6,351,163) and Takenaka (U.S. Patent No. 5,504,452).

C. Claims 3-4, 8, 14-18 and 31 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Naganuma (U.S. Patent No. 4,827,159) in view of Love (U.S. Patent No. 5,068,553).

D. Claim 19 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Naganuma (U.S. Patent No. 4,827,159) and Love (U.S. Patent No. 5,068,553) as applied to claim 18 and in view of Yoshizawa et al. (U.S. Patent No. 6,351,163) and Takenaka (U.S. Patent No. 5,504,452).

(7) ARGUMENT

Argument re Issue A

Claims 3-4, 6, 8-9, 11-18 and 25-31 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Naganuma (U.S. Patent No. 4,827,159) in view of Bui et al. (U.S. Patent No. 6,201,752). Appellants respectfully assert, for at least the reasons advanced below, that claims 3-4, 6, 8-9, 11-18 and 25-31 are not unpatentable over Naganuma (U.S. Patent No. 4,827,159) in view of Bui et al. (U.S. Patent No. 6,201,752).

Claims 3-4, 8-9, 11-18, 25, 31

Claim 31 recites the following:

A circuit comprising a first terminal for connection to a voltage source having first and second levels and a transition between the levels,

a driver including first and second opposite conductivity type transistors, each including a control electrode and a path arranged to be switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold level, the first and second transistor paths being connected in series across opposite power supply terminals, an output terminal between the paths, and circuitry connected between the first terminal and the control electrodes for causing the first and second transistor paths to be respectively (a) in on and off states while the voltage source has

the first level and (b) in off and on states while the voltage source has the second level,

wherein said circuitry includes at least one voltage responsive switchable capacitor connected (a) to be responsive to voltage at the first terminal and (b) to the driver for preventing the paths of the first and second transistors from being on simultaneously during transitions between the on and off states of the first and second transistor paths, the at least one switchable capacitor being arranged to have an initial finite capacitance value during an initial part of the transition between the levels and to be switched from the initial finite capacitance value to a substantially open circuit in response to the voltage across the at least one switchable capacitor changing during the transition between the levels from one side of a threshold voltage to a second side of the threshold voltage, the threshold voltage being between the first and second levels;

said at least one voltage responsive switchable capacitor has a capacitor control electrode connected to the control electrode of one of the first and second transistors to receive the voltage applied to the control electrode of said one of the first and second transistors;

the threshold voltage of said at least one voltage responsive switchable capacitor and the threshold level of said one of the first and second transistors are configured such that, as the voltage changes in a direction to switch said one of the first and second transistors from off to on, said one of the first and second transistors is switched from off to on before said at least one voltage responsive

switchable capacitor is switched from the initial finite capacitance value to the substantially open circuit; and

said at least one voltage responsive switchable capacitor is the only voltage responsive switchable capacitor connected to the control electrode of said one of the first and second transistors.

Claim 3 recites the following:

The circuit of claim 31 wherein the at least one switchable capacitor is connected between said one of the control electrodes and a DC power supply terminal of the circuit.

Claim 4 recites the following:

The circuit of claim 3 wherein the circuitry further includes a resistive element connected to supply current to the at least one switchable capacitor in response to the voltage at the first terminal.

Claim 8 recites the following:

The circuit of claim 31 wherein the at least one switchable capacitor includes first and second voltage controlled switchable capacitors respectively connected to delay coupling of the transitions to the control electrodes of the first and second transistors.

Claim 9 recites the following:

The circuit of claim 8 wherein said first and second capacitors are respectively connected between the control electrodes of the

transistors and the opposite power supply terminals are respectively first and second power supply terminals of the circuit and are such that (a) the first capacitor is arranged to have a finite capacitance value on a first side of a first voltage threshold and a substantially open circuit on a second side of the first threshold, and (b) the second capacitor is arranged to have a finite capacitance value on a second side of a second voltage threshold and a substantially open circuit on a first side of the second threshold, one of the first and second thresholds being higher than the other, and both the first and second thresholds being between the first and second levels.

Claim 11 recites the following:

The circuit of claim 9 wherein the circuitry further includes first and second resistive elements respectively connected to supply current to the first and second capacitors in response to the voltage at the first terminal.

Claim 12 recites the following:

The circuit of claim 11 wherein the first and second transistors are respectively a PFET and an NFET and the first and second capacitors are respectively an NFET and a PFET;

the threshold voltage of said first capacitor is lower than the threshold level of said first transistor; and

the threshold voltage of said second capacitor is higher than the threshold level of said second transistor.

Claim 13 recites the following:

The circuit of claim 12 wherein the first and second transistors, the first and second resistive elements, and the first and second capacitors are included on an integrated circuit chip, the first and second resistive elements including first and second resistors on the chip.

Claim 14 recites the following:

The circuit of claim 8 wherein the circuitry further includes first and second inverters each having (a) an input terminal for enabling the first and second inverters to be simultaneously responsive to the voltage at the first terminal and (b) an output terminal, the output terminal of the first inverter being connected to supply current via a first DC path to the first capacitor and the control electrode of the first transistor to the exclusion of the second capacitor and the control electrode of the second transistor, the output terminal of the second inverter being connected to supply current via a second DC path to the second capacitor and the control electrode of the second transistor to the exclusion of the first capacitor and the control electrode of the first transistor.

Claim 15 recites the following:

The circuit of claim 14 wherein the first and second transistors are field effect transistors, the first and second inverters comprise field effect transistors, and the first and second capacitors comprise

field effect transistors.

Claim 16 recites the following:

The circuit of claim 15 wherein all of the field effect transistors are included on an integrated circuit chip including first and second resistors respectively connected with the first and second transistors and the first and second inverters.

Claim 17 recites the following:

The circuit of claim 16 wherein the first and second resistors are respectively included in the first and second inverters.

Claim 18 recites the following:

The circuit of claim 8 wherein the first and second transistors are respectively a PFET and an NFET, the circuitry further includes first and second inverters, each of the first and second inverters having (a) an input terminal for enabling the first and second inverters to be simultaneously responsive to the voltage at the first terminal and (b) an output terminal, the output terminal of the first inverter being connected to supply current via a first DC path to the first capacitor and the control electrode of the first transistor, the output terminal of the second inverter being connected to supply current via a second DC path to the second capacitor and the control electrode of the second transistor, each of the inverters including a PFET and an NFET, the PFET and NFET of each inverter having a

source drain path and a gate electrode having a connection to the first terminal so that the gate electrodes of the PFETs and NFETs of the inverters are driven in parallel by the voltage at the input terminal, the output terminal of each of the inverters being between the source drain paths of the PFET and NFET thereof,

the first and second capacitors comprise field effect transistors,

all of the field effect transistors are included on an integrated circuit chip including first and second resistors respectively connected with the first and second field effect transistors and the first and second inverters, and

the first and second resistors are respectively included in the first and second inverters.

Claim 25 recites the following:

The circuit of claim 9, wherein the first and second transistors are respectively a PFET and an NFET and the first and second capacitors are respectively an NFET and a PFET, the first transistor having a source drain path connection to a positive power supply terminal, the second transistor having a source drain path connection to a negative power supply terminal, the positive and negative power supply terminals respectively being the first and second power supply terminals, the first capacitor having a first electrode connected to the gate electrode of the first transistor and a second electrode connected to the negative power supply terminal,

the second capacitor having a first electrode connected to the gate electrode of the second transistor and a second electrode connected to the positive power supply terminal;

the threshold voltage of said first capacitor is lower than the threshold level of said first transistor; and

the threshold voltage of said second capacitor is higher than the threshold level of said second transistor.

In Figure 1 of the application, a first switched voltage controlled shunt capacitor 32 (pg.4, line 19) is created using a PFET. The drain and the source of this PFET are connected to ground. The gate of the PFET is connected to node 28. When the gate is discharged to ground, the voltage controlled shunt capacitor 32 has nearly no capacitance because both plates of the capacitor 32 are at ground. As result when node 28 begins to charge, there is little capacitance and the node at this point in time may be charged quickly.

If an NFET switched voltage controlled shunt capacitor is added in parallel with switched voltage controlled shunt capacitor 32 at node 28, the time required to charge node 28 from ground to VDD will increase. Therefore it is not desirable to add an NFET switched voltage controlled shunt capacitor, as suggested by *Bui* and *Naganuma*, in parallel with the switched voltage controlled shunt capacitor 32 at node 28.

In Figure 1 of the application, a second switched voltage

controlled shunt capacitor 34 (pg.4, line 19) is created using an NFET. The drain and the source of this NFET are connected to VDD. The gate of the NFET is connected to node 30. When the gate is charged to VDD, the voltage controlled shunt capacitor 34 has nearly no capacitance because both plates of the capacitor 34 are at VDD. As a result when node 30 begins to discharge, there is little capacitance and the node at this point in time may be discharged quickly.

If a PFET switched voltage controlled shunt capacitor is added in parallel with switched voltage controlled shunt capacitor 34 at node 30, the time required to discharge node 30 from VDD to GND will increase. Therefore it is not desirable to add a PFET switched voltage controlled shunt capacitor, as suggest by *Bui* and *Naganuma*, in parallel with switched voltage controlled shunt capacitor 34 at node 30.

Appellants respectfully disagree with the Examiner's position that it would have been obvious to connect the *Bui* capacitors 807 and 808 separately to different nodes b) and c) of *Naganuma* because *Bui* expressly requires that the capacitors 807 and 808 be commonly connected to the same node as best seen in Fig. 8A of the reference. If both PFET and NFET switched voltage controlled shunt capacitors are commonly connected to the same node, the timing needed to reduce the amount of crow-bar current drawn from the power supply would be altered (See page 13, paragraph 26 of the application).

In addition, if both *Bui* capacitors 807 and 808 were connected to a control electrode of one of the first and second transistors, the resulting circuit would fail to teach or suggest the feature of claim 31 that "said at least one voltage responsive switchable capacitor is the **only** voltage responsive switchable capacitor connected to the control electrode of said one of the first and second transistors." The rejection, therefore, lacks a clear articulation of the reason(s) why it would have been obvious to separate the commonly connected capacitors 807 and 808 of *Bui*.

For at least the reasons above, Appellants respectfully assert that the current rejection of claim 31 is improper and should, therefore, be overruled. Therefore, Appellants respectfully request that the rejection of claim 31 be withdrawn.

Claims 3-4, 8-9, 11-18 and 25 are allowable at least as depending from allowable base claim 31. For purposes of this appeal, claims 3-4, 8-9, 11-18 and 25 stand or fall with claim 31.

Claims 6, 26-30

Claim 26 recites the following:

A driver having an input terminal adapted to be responsive to a bi-level signal, the driver including first and second opposite conductivity type transistors, each including a control electrode and a path between a pair of further electrodes controlled in response to a voltage applied to the control electrode, the paths of the first and second transistors being connected in series across opposite first and second power supply terminals, an output terminal between the

series connected paths, a first switchable capacitor connected to a first connection between the control electrode of the first transistor and the second power supply terminal, a second switchable capacitor connected to a second connection between the control electrode of the second transistor and the first power supply terminal, the first and second transistors having first and second thresholds between the voltages at the first and second power supply terminals so that the paths of the first and second transistors are arranged to be on and off in response to the voltages applied to the control electrodes being on opposite sides of the first and second thresholds thereof, the first and second capacitors respectively having third and fourth thresholds between the voltages at the first and second power supply terminals for causing the capacitors to have finite values and be switched off in response to the voltages across the capacitors being on opposite sides of the third and fourth thresholds;

the control electrodes and the capacitors being connected to each other and to the input terminal, the connections of the capacitors to the control electrode and to the input terminal and the first, second, third and fourth thresholds being such that in response to:

(I) a first transition between the levels of the bi-level signal that extends in a first direction, (a) the second capacitor is switched off and the voltage across the second capacitor and at the control electrode of the second transistor suddenly changes toward the voltage at the second power supply terminal in response to the

voltage across the second capacitor crossing the fourth threshold, (b) the first transistor is turned off and remains turned off until after a second transition between the levels of the bi-level signal that extends in a second direction, (c) the first capacitor has finite values until after the second transition, (d) the second transistor (i) is initially off while the first transistor is off, and (ii) then turns on in response to the voltage across the second capacitor and at the control electrode of the second transistor gradually changing in a direction extending from the voltage at the second power supply terminal toward the voltage at the first power supply terminal and crossing the second threshold, and (iii) stays on until the second transition occurs, wherein (a) occurs after (d)(ii); and

(II) the second transition, (a) the first capacitor is switched off and the voltage across the first capacitor and at the control electrode of the first transistor suddenly changes toward the voltage at the first power supply terminal in response to the voltage across the first capacitor crossing the third threshold, (b) the second transistor is turned off and remains turned off until after the first transition, (c) the second capacitor has finite values until after the first transition between the levels of the bi-level signal that extends in a second direction, (d) the first transistor (i) is initially off while the first transistor is off, and (ii) then turns on in response to the voltage across the first capacitor and at the control electrode of the first transistor gradually changing in a direction extending from the voltage at the second power supply terminal toward the voltage at the first power supply terminal and crossing the first threshold, and

(iii) stays on until the first transition occurs, wherein (a) occurs after (d)(ii);

wherein said first switchable capacitor is the only voltage responsive switchable capacitor directly connected to said first connection; and

said second switchable capacitor is the only voltage responsive switchable capacitor directly connected to said second connection.

Claim 27 recites the following:

The driver of claim 26, wherein the first and second transistors are respectively a PFET and an NFET, the first and second capacitors are respectively N and P doped FET devices, and the voltages adapted to be connected to the first and second power supply terminals are respectively positive and negative relative to each other, the N doped FET capacitor device being connected so it does not affect current flowing between the input terminal and the gate electrode of the NFET second transistor and the P doped FET capacitor device being connected so it does not affect current flowing between the input terminal and the gate electrode of the PFET first transistor.

Claim 28 recites the following:

The driver of claim 26 wherein said first and second transistors are respectively a PFET and an NFET, the opposite power supply terminals being respectively first and second power supply terminals,

the first power supply terminal being adapted to be connected to a voltage having a higher value than the voltage adapted to be connected to the second power supply terminal, said second switchable capacitor comprising a PFET having (a) a gate electrode connected to the gate electrode of the NFET second transistor, (b) a source electrode, and (c) a drain electrode, the source and drain electrodes of the PFET switchable capacitor being connected to the first power supply terminal, the PFET capacitor being connected so it does not affect current flowing between the input terminal and the gate of the PFET first transistor.

Claim 6 recites the following:

The circuit of claim 28, wherein the circuitry further includes a resistive element connected to supply current to one of the first and second switchable capacitors in response to the voltage at the first terminal, wherein said PFET of said driver, said NFET of said driver and said first and second switchable capacitors are included on an integrated circuit chip, and said resistive element comprises a resistor.

Claim 29 recites the following:

The driver of claim 26 wherein said first and second transistors are respectively a PFET and an NFET, the opposite power supply terminals being respectively first and second power supply terminals, the first power supply terminal being adapted to be connected to a voltage having a higher value than the voltage adapted to be

connected to the second power supply terminal, said first switchable capacitor comprising an NFET having (a) a gate electrode connected to the gate electrode of the PFET first transistor, (b) a source electrode, and (c) a drain electrode, the source and drain electrodes of the NFET capacitor being connected to the second power supply terminal, the NFET capacitor being connected so it does not affect current flowing between the input terminal and the gate of the NFET second transistor.

Claim 30 recites the following:

The driver of claim 29 wherein said second switchable capacitor comprises a PFET having (a) a gate electrode connected to the gate electrode of the NFET second transistor, (b) a source electrode, and (c) a drain electrode, the source and drain electrodes of the PFET capacitor being connected to the first power supply terminal, the PFET capacitor being connected so it does not affect current flowing between the input terminal and the gate of the PFET first transistor.

Regarding claim 26, Appellants respectfully assert that the current rejection of claim 26 is improper and should, for the same reasons given for claim 31 above, be overruled. Therefore, Appellants respectfully requests that the rejection of claim 26 be withdrawn.

Claims 6 and 27-30 are allowable at least as depending from allowable base claim 26. For purposes of this appeal, claims 6 and

27-30 stand or fall with claim 26.

Argument re Issue B

Claims 19-21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Naganuma (U.S. Patent No. 4,827,159) and Bui (U.S. Patent No. 6,201,752) as applied to claim 18 and in view of Yoshizawa et al. (U.S. Patent No. 6,351,163) and Takenaka (U.S. Patent No. 5,504,452). Appellants respectfully assert, for at least the reasons advanced below, that claims 19-21 are not unpatentable over Naganuma (U.S. Patent No. 4,827,159) and Bui (U.S. Patent No. 6,201,752) as applied to claim 18 and in view of Yoshizawa et al. (U.S. Patent No. 6,351,163) and Takenaka (U.S. Patent No. 5,504,452).

Claims 19-21

Claim 19 recites the following:

The circuit of claim 18 wherein the first resistor is connected between the source drain path of the NFET of the first inverter and the output terminal of the first inverter, and

the second resistor is connected between the source drain path of the PFET of the second inverter and the output terminal of the second inverter.

Claim 31 recites the following:

A circuit comprising a first terminal for connection to a voltage source having first and second levels and a transition between the levels,

a driver including first and second opposite conductivity type

transistors, each including a control electrode and a path arranged to be switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold level, the first and second transistor paths being connected in series across opposite power supply terminals, an output terminal between the paths, and circuitry connected between the first terminal and the control electrodes for causing the first and second transistor paths to be respectively (a) in on and off states while the voltage source has the first level and (b) in off and on states while the voltage source has the second level,

wherein said circuitry includes at least one voltage responsive switchable capacitor connected (a) to be responsive to voltage at the first terminal and (b) to the driver for preventing the paths of the first and second transistors from being on simultaneously during transitions between the on and off states of the first and second transistor paths, the at least one switchable capacitor being arranged to have an initial finite capacitance value during an initial part of the transition between the levels and to be switched from the initial finite capacitance value to a substantially open circuit in response to the voltage across the at least one switchable capacitor changing during the transition between the levels from one side of a threshold voltage to a second side of the threshold voltage, the threshold voltage being between the first and second levels;

said at least one voltage responsive switchable capacitor has a capacitor control electrode connected to the control electrode of one of the first and second transistors to receive the voltage applied to

the control electrode of said one of the first and second transistors;

the threshold voltage of said at least one voltage responsive switchable capacitor and the threshold level of said one of the first and second transistors are configured such that, as the voltage changes in a direction to switch said one of the first and second transistors from off to on, said one of the first and second transistors is switched from off to on before said at least one voltage responsive switchable capacitor is switched from the initial finite capacitance value to the substantially open circuit; and

said at least one voltage responsive switchable capacitor is the only voltage responsive switchable capacitor connected to the control electrode of said one of the first and second transistors.

Claim 20 recites the following:

The circuit of claim 19 wherein the first and second capacitors respectively include an NFET and a PFET;

the threshold voltage of said first capacitor is lower than the threshold level of said first transistor; and

the threshold voltage of said second capacitor is higher than the threshold level of said second transistor.

Claim 21 recites the following:

The circuit of claim 20 wherein the NFET and PFET included in the first and second capacitors respectively have different first and second thresholds between the first and second levels, the NFET included in the first capacitor having a finite capacitance value for

voltages above the first threshold and being a substantially open circuit for voltages lower than the first threshold, the PFET included in the second capacitor having a finite capacitance value for voltages lower than the second threshold and being a substantially open circuit for voltages above the second threshold, the first threshold being lower than the second threshold.

Claims 19-21 are allowable at least as depending from allowable base claim 31. For purposes of this appeal, claims 19-21 stand or fall with claim 31.

Argument re Issue C

Claims 3-4, 8, 14-18 and 31 stand rejected under 35 U.S.C.

103(a) as being unpatentable over Naganuma (U.S. Patent No. 4,827,159) in view of Love (U.S. Patent No. 5,068,553). Appellants respectfully assert, for at least the reasons advanced below, that claims 3-4, 8, 14-18 and 31 are not unpatentable over Naganuma (U.S. Patent No. 4,827,159) in view of Love (U.S. Patent No. 5,068,553).

Claims 3-4, 8, 14-18 & 31

Claim 31 recites the following:

A circuit comprising a first terminal for connection to a voltage source having first and second levels and a transition between the levels,

a driver including first and second opposite conductivity type transistors, each including a control electrode and a path arranged to be switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold level, the first and second transistor paths being connected in series across opposite power supply terminals, an output terminal between the paths, and circuitry connected between the first terminal and the control electrodes for causing the first and second transistor paths to be respectively (a) in on and off states while the voltage source has the first level and (b) in off and on states while the voltage source has the second level,

wherein said circuitry includes at least one voltage responsive switchable capacitor connected (a) to be responsive to voltage at the

first terminal and (b) to the driver for preventing the paths of the first and second transistors from being on simultaneously during transitions between the on and off states of the first and second transistor paths, the at least one switchable capacitor being arranged to have an initial finite capacitance value during an initial part of the transition between the levels and to be switched from the initial finite capacitance value to a substantially open circuit in response to the voltage across the at least one switchable capacitor changing during the transition between the levels from one side of a threshold voltage to a second side of the threshold voltage, the threshold voltage being between the first and second levels;

said at least one voltage responsive switchable capacitor has a capacitor control electrode connected to the control electrode of one of the first and second transistors to receive the voltage applied to the control electrode of said one of the first and second transistors;

the threshold voltage of said at least one voltage responsive switchable capacitor and the threshold level of said one of the first and second transistors are configured such that, as the voltage changes in a direction to switch said one of the first and second transistors from off to on, said one of the first and second transistors is switched from off to on before said at least one voltage responsive switchable capacitor is switched from the initial finite capacitance value to the substantially open circuit; and

said at least one voltage responsive switchable capacitor is the only voltage responsive switchable capacitor connected to the control electrode of said one of the first and second transistors.

Claim 3 recites the following:

The circuit of claim 31 wherein the at least one switchable capacitor is connected between said one of the control electrodes and a DC power supply terminal of the circuit.

Claim 4 recites the following:

The circuit of claim 3 wherein the circuitry further includes a resistive element connected to supply current to the at least one switchable capacitor in response to the voltage at the first terminal.

Claim 8 recites the following:

The circuit of claim 31 wherein the at least one switchable capacitor includes first and second voltage controlled switchable capacitors respectively connected to delay coupling of the transitions to the control electrodes of the first and second transistors.

Claim 14 recites the following:

The circuit of claim 8 wherein the circuitry further includes first and second inverters each having (a) an input terminal for enabling the first and second inverters to be simultaneously responsive to the voltage at the first terminal and (b) an output terminal, the output terminal of the first inverter being connected to supply current via a first DC path to the first capacitor and the control electrode of the first transistor to the exclusion of the second capacitor and the control electrode of the second transistor, the output terminal of the

second inverter being connected to supply current via a second DC path to the second capacitor and the control electrode of the second transistor to the exclusion of the first capacitor and the control electrode of the first transistor.

Claim 15 recites the following:

The circuit of claim 14 wherein the first and second transistors are field effect transistors, the first and second inverters comprise field effect transistors, and the first and second capacitors comprise field effect transistors.

Claim 16 recites the following:

The circuit of claim 15 wherein all of the field effect transistors are included on an integrated circuit chip including first and second resistors respectively connected with the first and second transistors and the first and second inverters.

Claim 17 recites the following:

The circuit of claim 16 wherein the first and second resistors are respectively included in the first and second inverters.

Claim 18 recites the following:

The circuit of claim 8 wherein the first and second transistors are respectively a PFET and an NFET, the circuitry further includes first and second inverters, each of the first and second inverters having (a) an input terminal for enabling the first and second

inverters to be simultaneously responsive to the voltage at the first terminal and (b) an output terminal, the output terminal of the first inverter being connected to supply current via a first DC path to the first capacitor and the control electrode of the first transistor, the output terminal of the second inverter being connected to supply current via a second DC path to the second capacitor and the control electrode of the second transistor, each of the inverters including a PFET and an NFET, the PFET and NFET of each inverter having a source drain path and a gate electrode having a connection to the first terminal so that the gate electrodes of the PFETs and NFETs of the inverters are driven in parallel by the voltage at the input terminal, the output terminal of each of the inverters being between the source drain paths of the PFET and NFET thereof,

the first and second capacitors comprise field effect transistors,

all of the field effect transistors are included on an integrated circuit chip including first and second resistors respectively connected with the first and second field effect transistors and the first and second inverters, and

the first and second resistors are respectively included in the first and second inverters.

With respect to claim 31, the Appellants respectfully disagree with the Examiner's position that it would have been obvious to combine *Naganuma* with *Love*. The delay element of *Love*, i.e., capacitor 80, is provided between stages, 78, 90, i.e., within an

inverter. The *Love* reference does not supply any teaching or suggestion of providing a delay stage after or downstream of the inverter. *Naganuma* discloses an inverter at 51, 52. A person of ordinary skill in the art learning of the teachings of *Naganuma* and *Love* would have included, if at all, the *Love* delay stage within the *Naganuma* inverter 51, 52, rather than downstream thereof as proposed by the Examiner.

In addition, the Examiner's proposed combination, if at all proper, would include a NMOS capacitor where a PMOS capacitor is required, and *vice versa*. The Examiner's proposed combination would still be different from the claimed invention. It is unclear why it would have been obvious to further modify the NMOS capacitor imported from *Love* into a PMOS capacitor to arrive, if at all, at the claimed invention.

Finally, the NMOS vs. PMOS difference is not a minor one, contrary to the Examiner's position. It should be noted that NMOS capacitor 80 of *Love* is provided to limit the rising speed of the signal at node 76. The reference also discloses how to limit the falling speed of the signal at node 76, by moving the resistor 72 to the branch associated with transistor 70 and apparently, by additionally changing the capacitor to a PMOS capacitor. Thus, *Love* clearly discloses that the polarity of capacitor 80 cannot be arbitrarily set; rather, the reference requires that the polarity of capacitor 80 must be specifically chosen to provide appropriate rising/falling speed limiting action. Given the above overall teaching of *Love*, a person of ordinary skill in the art, if at all motivated, would have combined

Naganuma and *Love* with a NMOS capacitor 80, instead of a PMOS capacitor. The person of ordinary skill in the art would not have been motivated to further change the NMOS capacitor to a PMOS capacitor because such further modification would fail to limit the rising speed at the output c) of the *Naganuma* inverter, and hence, would defeat the intended purpose of inserting the *Love* capacitor 80 into the *Naganuma* circuit.

For at least the reasons above, Appellants respectfully assert that the current rejection of claim 31 is improper and should, therefore, be overruled. Therefore, Appellants respectfully request that the rejection of claim 31 be withdrawn.

Claims 3-4, 8 and 14-18 are allowable at least as depending from allowable base claim 31. For purposes of this appeal, claims 3-4, 8 and 14-18 stand or fall with claim 31.

Argument re Issue D

Claim 19 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Naganuma (U.S. Patent No. 4,827,159) and Love (U.S. Patent No. 5,068,553) as applied to claim 18 and in view of Yoshizawa et al. (U.S. Patent No. 6,351,163) and Takenaka (U.S. Patent No. 5,504,452). Appellants respectfully assert, for at least the reasons advanced below, that claim 19 is not unpatentable over Naganuma (U.S. Patent No. 4,827,159) and Love (U.S. Patent No. 5,068,553) as applied to claim 18 and in view of Yoshizawa et al. (U.S. Patent No. 6,351,163) and Takenaka (U.S. Patent No. 5,504,452).

Claim 19

Claim 19 recites the following:

The circuit of claim 18 wherein the first resistor is connected between the source drain path of the NFET of the first inverter and the output terminal of the first inverter, and

the second resistor is connected between the source drain path of the PFET of the second inverter and the output terminal of the second inverter.

Claim 31 recites the following:

A circuit comprising a first terminal for connection to a voltage source having first and second levels and a transition between the levels,

a driver including first and second opposite conductivity type

transistors, each including a control electrode and a path arranged to be switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold level, the first and second transistor paths being connected in series across opposite power supply terminals, an output terminal between the paths, and circuitry connected between the first terminal and the control electrodes for causing the first and second transistor paths to be respectively (a) in on and off states while the voltage source has the first level and (b) in off and on states while the voltage source has the second level,

wherein said circuitry includes at least one voltage responsive switchable capacitor connected (a) to be responsive to voltage at the first terminal and (b) to the driver for preventing the paths of the first and second transistors from being on simultaneously during transitions between the on and off states of the first and second transistor paths, the at least one switchable capacitor being arranged to have an initial finite capacitance value during an initial part of the transition between the levels and to be switched from the initial finite capacitance value to a substantially open circuit in response to the voltage across the at least one switchable capacitor changing during the transition between the levels from one side of a threshold voltage to a second side of the threshold voltage, the threshold voltage being between the first and second levels;

said at least one voltage responsive switchable capacitor has a capacitor control electrode connected to the control electrode of one of the first and second transistors to receive the voltage applied to

the control electrode of said one of the first and second transistors;

the threshold voltage of said at least one voltage responsive switchable capacitor and the threshold level of said one of the first and second transistors are configured such that, as the voltage changes in a direction to switch said one of the first and second transistors from off to on, said one of the first and second transistors is switched from off to on before said at least one voltage responsive switchable capacitor is switched from the initial finite capacitance value to the substantially open circuit; and

said at least one voltage responsive switchable capacitor is the only voltage responsive switchable capacitor connected to the control electrode of said one of the first and second transistors.

Claim 19 is allowable at least as depending from allowable base claim 31. For purposes of this appeal, claim 19 stands or falls with claim 31.

Respectfully submitted,
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(8) CLAIMS APPENDIX

1-2. (Canceled)

3. The circuit of claim 31 wherein the at least one switchable capacitor is connected between said one of the control electrodes and a DC power supply terminal of the circuit.

4. The circuit of claim 3 wherein the circuitry further includes a resistive element connected to supply current to the at least one switchable capacitor in response to the voltage at the first terminal.

5. (Canceled)

6. The circuit of claim 28, wherein the circuitry further includes a resistive element connected to supply current to one of the first and second switchable capacitors in response to the voltage at the first terminal, wherein said PFET of said driver, said NFET of said driver and said first and second switchable capacitors are included on an integrated circuit chip, and said resistive element comprises a resistor.

7. (Canceled)

8. The circuit of claim 31 wherein the at least one switchable capacitor includes first and second voltage controlled switchable capacitors respectively connected to delay coupling of the transitions to the control electrodes of the first and second transistors.

9. The circuit of claim 8 wherein said first and second capacitors are respectively connected between the control electrodes of the transistors and the opposite power supply terminals are respectively first and second power supply terminals of the circuit and are such that (a) the first capacitor is arranged to have a finite capacitance value on a first side of a first voltage threshold and a substantially open circuit on a second side of the first threshold, and (b) the second capacitor is arranged to have a finite capacitance value on a second side of a second voltage threshold and a substantially open circuit on a first side of the second threshold, one of the first and second thresholds being higher than the other, and both the first and second thresholds being between the first and second levels.

10. (Canceled)

11. The circuit of claim 9 wherein the circuitry further includes first and second resistive elements respectively connected to supply current to the first and second capacitors in response to the voltage at the first terminal.

12. The circuit of claim 11 wherein the first and second transistors are respectively a PFET and an NFET and the first and second capacitors are respectively an NFET and a PFET;

the threshold voltage of said first capacitor is lower than the threshold level of said first transistor; and

the threshold voltage of said second capacitor is higher than the threshold level of said second transistor.

13. The circuit of claim 12 wherein the first and second transistors, the first and second resistive elements, and the first and second capacitors are included on an integrated circuit chip, the first and second resistive elements including first and second resistors on the chip.

14. The circuit of claim 8 wherein the circuitry further includes first and second inverters each having (a) an input terminal for enabling the first and second inverters to be simultaneously responsive to the voltage at the first terminal and (b) an output terminal, the output terminal of the first inverter being connected to supply current via a first DC path to the first capacitor and the control electrode of the first transistor to the exclusion of the second capacitor and the control electrode of the second transistor, the output terminal of the second inverter being connected to supply current via a second DC path to the second capacitor and the control electrode of the second transistor to the exclusion of the first

capacitor and the control electrode of the first transistor.

15. The circuit of claim 14 wherein the first and second transistors are field effect transistors, the first and second inverters comprise field effect transistors, and the first and second capacitors comprise field effect transistors.

16. The circuit of claim 15 wherein all of the field effect transistors are included on an integrated circuit chip including first and second resistors respectively connected with the first and second transistors and the first and second inverters.

17. The circuit of claim 16 wherein the first and second resistors are respectively included in the first and second inverters.

18. The circuit of claim 8 wherein the first and second transistors are respectively a PFET and an NFET, the circuitry further includes first and second inverters, each of the first and second inverters having (a) an input terminal for enabling the first and second inverters to be simultaneously responsive to the voltage at the first terminal and (b) an output terminal, the output terminal of the first inverter being connected to supply current via a first DC path to the first capacitor and the control electrode of the first transistor, the output terminal of the second inverter being connected to supply current via a second DC path to the second capacitor and the control

electrode of the second transistor, each of the inverters including a PFET and an NFET, the PFET and NFET of each inverter having a source drain path and a gate electrode having a connection to the first terminal so that the gate electrodes of the PFETs and NFETs of the inverters are driven in parallel by the voltage at the input terminal, the output terminal of each of the inverters being between the source drain paths of the PFET and NFET thereof,

the first and second capacitors comprise field effect transistors,

all of the field effect transistors are included on an integrated circuit chip including first and second resistors respectively connected with the first and second field effect transistors and the first and second inverters, and

the first and second resistors are respectively included in the first and second inverters.

19. The circuit of claim 18 wherein the first resistor is connected between the source drain path of the NFET of the first inverter and the output terminal of the first inverter, and

the second resistor is connected between the source drain path of the PFET of the second inverter and the output terminal of the second inverter.

20. The circuit of claim 19 wherein the first and second

capacitors respectively include an NFET and a PFET;

the threshold voltage of said first capacitor is lower than the threshold level of said first transistor; and

the threshold voltage of said second capacitor is higher than the threshold level of said second transistor.

21. The circuit of claim 20 wherein the NFET and PFET included in the first and second capacitors respectively have different first and second thresholds between the first and second levels, the NFET included in the first capacitor having a finite capacitance value for voltages above the first threshold and being a substantially open circuit for voltages lower than the first threshold, the PFET included in the second capacitor having a finite capacitance value for voltages lower than the second threshold and being a substantially open circuit for voltages above the second threshold, the first threshold being lower than the second threshold.

22. A method of operating a driver including first and second opposite conductivity type transistors, each including a control electrode and a path between a pair of further electrodes controlled in response to a voltage applied to the control electrode, the paths of the first and second transistors being connected in series across opposite first and second power supply terminals, an output terminal between the series connected paths, a first switchable capacitor connected between the control electrode of the first transistor and

the first power supply terminal and a second switchable capacitor connected between the control electrode of the second transistor and the second power supply terminal, the method comprising:

during a first interval: causing the paths of the first and second transistors to be respectively, on and off by applying

(a) a first voltage having a first value to the control electrode of the first transistor,

(b) a second voltage having the first value to the control electrode of the second transistor and across the second capacitor to charge the second capacitor;

during a second interval: causing the paths of the first and second transistors to be off and on, respectively, by applying

(a) a second value of the first voltage to the control electrode of the first transistor, and

(b) the second value of the second voltage to the control electrode of the second transistor and across the first capacitor to charge the first capacitor;

upon a first transition between the first and second intervals: turning off, without any capacitive delay, the path of the first transistor while maintaining, during said first transition and during an initial portion of the second interval, the path of the second transistor off by changing the first voltage from the first value to the second value while the first capacitor is switched off and the second capacitor is charged;

after the initial portion of said second interval and during a

second, subsequent portion of the second interval: turning on the path of the second transistor while maintaining the path of the first transistor off by changing the charge on the second capacitor so that the second voltage changes from the first value toward the second value;

after the second portion of said second interval and during a third, subsequent portion of the second interval: while maintaining the paths of the second transistor and the first transistor on and off, respectively, switching off the second capacitor to cause the second voltage to reach the second value before a subsequent second transition between the second and first intervals;

upon the second transition between the second and first intervals: turning off, without ant capacitive delay, the path of the second transistor while maintaining, during said second transition and during an initial portion of the first interval, the path of the first transistor off by changing the second voltage from the second value to the first value while the second capacitor remains switched off and the first capacitor is charged;

after the initial portion of said first interval and during a second, subsequent portion of the first interval : turning on the path of the first transistor while maintaining the path of the second transistor off by changing the charge on the first capacitor so that the first voltage changes from the second value toward the first value; and

after the second portion of said first interval and during a third, subsequent portion of the first interval: while maintaining the paths of

the first transistor and the second transistor on and off, respectively, switching off the first capacitor to cause the first voltage to reach the first value before the subsequent first transition between the second and first intervals.

23. (Canceled)

24. The method of claim 22 wherein the first and second capacitors are charged and switched off in response to the first and second voltages having values on opposite sides of first and second thresholds respectively associated with the first and second capacitors.

25. The circuit of claim 9, wherein the first and second transistors are respectively a PFET and an NFET and the first and second capacitors are respectively an NFET and a PFET, the first transistor having a source drain path connection to a positive power supply terminal, the second transistor having a source drain path connection to a negative power supply terminal, the positive and negative power supply terminals respectively being the first and second power supply terminals, the first capacitor having a first electrode connected to the gate electrode of the first transistor and a second electrode connected to the negative power supply terminal, the second capacitor having a first electrode connected to the gate electrode of the second transistor and a second electrode connected

to the positive power supply terminal;

the threshold voltage of said first capacitor is lower than the threshold level of said first transistor; and

the threshold voltage of said second capacitor is higher than the threshold level of said second transistor.

26. A driver having an input terminal adapted to be responsive to a bi-level signal, the driver including first and second opposite conductivity type transistors, each including a control electrode and a path between a pair of further electrodes controlled in response to a voltage applied to the control electrode, the paths of the first and second transistors being connected in series across opposite first and second power supply terminals, an output terminal between the series connected paths, a first switchable capacitor connected to a first connection between the control electrode of the first transistor and the second power supply terminal, a second switchable capacitor connected to a second connection between the control electrode of the second transistor and the first power supply terminal, the first and second transistors having first and second thresholds between the voltages at the first and second power supply terminals so that the paths of the first and second transistors are arranged to be on and off in response to the voltages applied to the control electrodes being on opposite sides of the first and second thresholds thereof, the first and second capacitors respectively having third and fourth thresholds between the voltages

at the first and second power supply terminals for causing the capacitors to have finite values and be switched off in response to the voltages across the capacitors being on opposite sides of the third and fourth thresholds;

the control electrodes and the capacitors being connected to each other and to the input terminal, the connections of the capacitors to the control electrode and to the input terminal and the first, second, third and fourth thresholds being such that in response to:

(I) a first transition between the levels of the bi-level signal that extends in a first direction, (a) the second capacitor is switched off and the voltage across the second capacitor and at the control electrode of the second transistor suddenly changes toward the voltage at the second power supply terminal in response to the voltage across the second capacitor crossing the fourth threshold, (b) the first transistor is turned off and remains turned off until after a second transition between the levels of the bi-level signal that extends in a second direction, (c) the first capacitor has finite values until after the second transition, (d) the second transistor (i) is initially off while the first transistor is off, and (ii) then turns on in response to the voltage across the second capacitor and at the control electrode of the second transistor gradually changing in a direction extending from the voltage at the second power supply terminal toward the voltage at the first power supply terminal and crossing the second threshold, and (iii) stays on until the second transition occurs,

wherein (a) occurs after (d)(ii); and

(II) the second transition, (a) the first capacitor is switched off and the voltage across the first capacitor and at the control electrode of the first transistor suddenly changes toward the voltage at the first power supply terminal in response to the voltage across the first capacitor crossing the third threshold, (b) the second transistor is turned off and remains turned off until after the first transition, (c) the second capacitor has finite values until after the first transition between the levels of the bi-level signal that extends in a second direction, (d) the first transistor (i) is initially off while the first transistor is off, and (ii) then turns on in response to the voltage across the first capacitor and at the control electrode of the first transistor gradually changing in a direction extending from the voltage at the second power supply terminal toward the voltage at the first power supply terminal and crossing the first threshold, and (iii) stays on until the first transition occurs, wherein (a) occurs after (d)(ii);

wherein said first switchable capacitor is the only voltage responsive switchable capacitor directly connected to said first connection; and

said second switchable capacitor is the only voltage responsive switchable capacitor directly connected to said second connection.

27. The driver of claim 26, wherein the first and second transistors are respectively a PFET and an NFET, the first and second capacitors are respectively N and P doped FET devices, and the voltages adapted to be connected to the first and second power supply terminals are respectively positive and negative relative to each other, the N doped FET capacitor device being connected so it does not affect current flowing between the input terminal and the gate electrode of the NFET second transistor and the P doped FET capacitor device being connected so it does not affect current flowing between the input terminal and the gate electrode of the PFET first transistor.

28. The driver of claim 26 wherein said first and second transistors are respectively a PFET and an NFET, the opposite power supply terminals being respectively first and second power supply terminals, the first power supply terminal being adapted to be connected to a voltage having a higher value than the voltage adapted to be connected to the second power supply terminal, said second switchable capacitor comprising a PFET having (a) a gate electrode connected to the gate electrode of the NFET second transistor, (b) a source electrode, and (c) a drain electrode, the source and drain electrodes of the PFET switchable capacitor being connected to the first power supply terminal, the PFET capacitor being connected so it does not affect current flowing between the input terminal and the gate of the PFET first transistor.

29. The driver of claim 26 wherein said first and second transistors are respectively a PFET and an NFET, the opposite power supply terminals being respectively first and second power supply terminals, the first power supply terminal being adapted to be connected to a voltage having a higher value than the voltage adapted to be connected to the second power supply terminal, said first switchable capacitor comprising an NFET having (a) a gate electrode connected to the gate electrode of the PFET first transistor, (b) a source electrode, and (c) a drain electrode, the source and drain electrodes of the NFET capacitor being connected to the second power supply terminal, the NFET capacitor being connected so it does not affect current flowing between the input terminal and the gate of the NFET second transistor.

30. The driver of claim 29 wherein said second switchable capacitor comprises a PFET having (a) a gate electrode connected to the gate electrode of the NFET second transistor, (b) a source electrode, and (c) a drain electrode, the source and drain electrodes of the PFET capacitor being connected to the first power supply terminal, the PFET capacitor being connected so it does not affect current flowing between the input terminal and the gate of the PFET first transistor.

31. A circuit comprising a first terminal for connection to a voltage source having first and second levels and a transition between the levels,

a driver including first and second opposite conductivity type transistors, each including a control electrode and a path arranged to be switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold level, the first and second transistor paths being connected in series across opposite power supply terminals, an output terminal between the paths, and circuitry connected between the first terminal and the control electrodes for causing the first and second transistor paths to be respectively (a) in on and off states while the voltage source has the first level and (b) in off and on states while the voltage source has the second level,

wherein said circuitry includes at least one voltage responsive switchable capacitor connected (a) to be responsive to voltage at the first terminal and (b) to the driver for preventing the paths of the first and second transistors from being on simultaneously during transitions between the on and off states of the first and second transistor paths, the at least one switchable capacitor being arranged to have an initial finite capacitance value during an initial part of the transition between the levels and to be switched from the initial finite capacitance value to a substantially open circuit in response to the voltage across the at least one switchable capacitor changing during the transition between the levels from one side of a

threshold voltage to a second side of the threshold voltage, the threshold voltage being between the first and second levels;

said at least one voltage responsive switchable capacitor has a capacitor control electrode connected to the control electrode of one of the first and second transistors to receive the voltage applied to the control electrode of said one of the first and second transistors;

the threshold voltage of said at least one voltage responsive switchable capacitor and the threshold level of said one of the first and second transistors are configured such that, as the voltage changes in a direction to switch said one of the first and second transistors from off to on, said one of the first and second transistors is switched from off to on before said at least one voltage responsive switchable capacitor is switched from the initial finite capacitance value to the substantially open circuit; and

said at least one voltage responsive switchable capacitor is the only voltage responsive switchable capacitor connected to the control electrode of said one of the first and second transistors.

(9) EVIDENCE APPENDIX

No evidence pursuant to §§ 1.130, 1.131 or 1.132 or entered by or relied upon by the Examiner is being submitted.

(10) RELATED PROCEEDINGS APPENDIX

No related proceedings are referenced in (2) above.

Accordingly, no copies of decisions in related proceedings are provided.